CDB5381

Evaluation Board for CS5381

Features

- Demonstrates recommended layout and grounding arrangements
- CS8406 generates S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

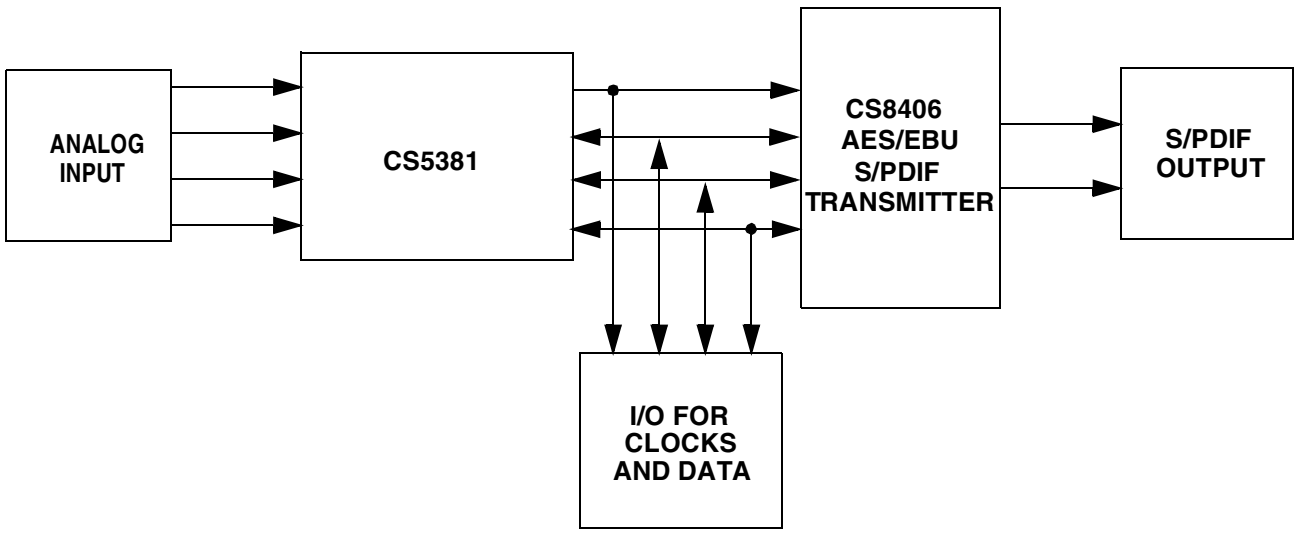
Description

The CDB5381 evaluation board is an excellent means for quickly evaluating the CS5381 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8406 digital audio interface transmitter which generates S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5381	Evaluation Board



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Contacting Cirrus Logic Support

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To find one nearest you go to **www.cirrus.com**

1. CDB5381 SYSTEM OVERVIEW

The CDB5381 evaluation board is an excellent means of quickly evaluating the CS5381. The CS8406 digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5381 schematic has been partitioned into 7 schematics shown in Figure 2 through Figure 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS8406 DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8406 Digital Audio Transmitter (see Figure 6). The outputs of the CS8406 are RS422 compatible differential line drivers. The CS8406 supports both Left Justified and I^2S data formats, as determined by the DIP switch, S2. A description of the CS8406 is included in the CS8406 datasheet.

3. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J13. The schematic for the clock/data input/output is shown in Figure 5.

The CDB5381 allows some flexibility as to the generation of the clocks. When the CS5381 and CS8406 are in slave mode, the SCLK and LRCK must be provided via the header, J13. MCLK must be generated from the on board oscillator, Y1. This oscillator is socketed to allow other frequency oscillators to be used.

4. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts (-12 V, +12 V, VD, VL, GND, +5 V), see Figure 8. -12 V and +12 V supply the input amplifiers while the VD input supplies the VD pin of the CS5381. VL supplies power to the VL pin of the CS5381 and to the level shifter circuits. The +5 V input supplies power to the +5 V digital circuitry and the VA pin of the CS5381.

5. GROUNDING AND POWER SUPPLY DECOUPLING

The CS5381 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5381 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

6. ANALOG INPUT FILTER

The CDB5381 implements a fully differential analog input buffer, as shown in Figure 2. Note that there is no attenuation associated with the input buffer, so a 2 Vrms differential input applied at the XLR connectors will provide a full-scale 2 Vrms differential input to the CS5381.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
-12 V	Input	-12 V power for the input op-amps
+12 V	Input	+12 V power for the input op-amps
VD	Input	+3.3 V to +5 V power for the CS5381
VL	Input	+2.5 V to +5 V power for the CS5381
GND	Input	Ground connection from power supply
+5 V	Input	+ 5 Volt power
AINL	Input	Differential analog input left channel
AINR	Input	Differential analog input right channel
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER/SWITCH	PURPOSE	POSITION		FUNCTION SELECTED
J7	VD Power Source	ADJ *+3.3 V +5 V		Power from the Binding Post (J3) Power from the +3.3 V Regulator Power from the +5V Supply
J8	VL Power Source	ADJ *+3.3 V +5 V		Power from the Binding Post (J4) Power from the +3.3 V Regulator Power from the +5 V Supply
J13	Input/Output for clocks/data	-		-
S1	Reset for the CDB5381	-		-
S2	CDB5381 Configuration	M1/M0	Open *Closed	Hi Low
		ADC	*Open Closed	CS5381 in Master mode CS5381 in Slave mode
		$\overline{\text{HPF}}$	Open *Closed	High-pass filter is disabled High-pass filter is enabled
		DIV	Open *Closed	MCLK is divided by two internally by the CS5381 MCLK is not divided internally by the CS5381
		IO_HDR	Open *Closed	Header J3 is an input for clocks Header J3 is an output for clocks and data
		DIF	Open *Closed	Digital interface format set to I^2S Digital interface format set to Left Justified
		8406	Open *Closed	CS8406 in Master mode CS8406 in Slave mode

Table 2. CDB5381 Jumper and Switch Settings

* denotes default factory settings

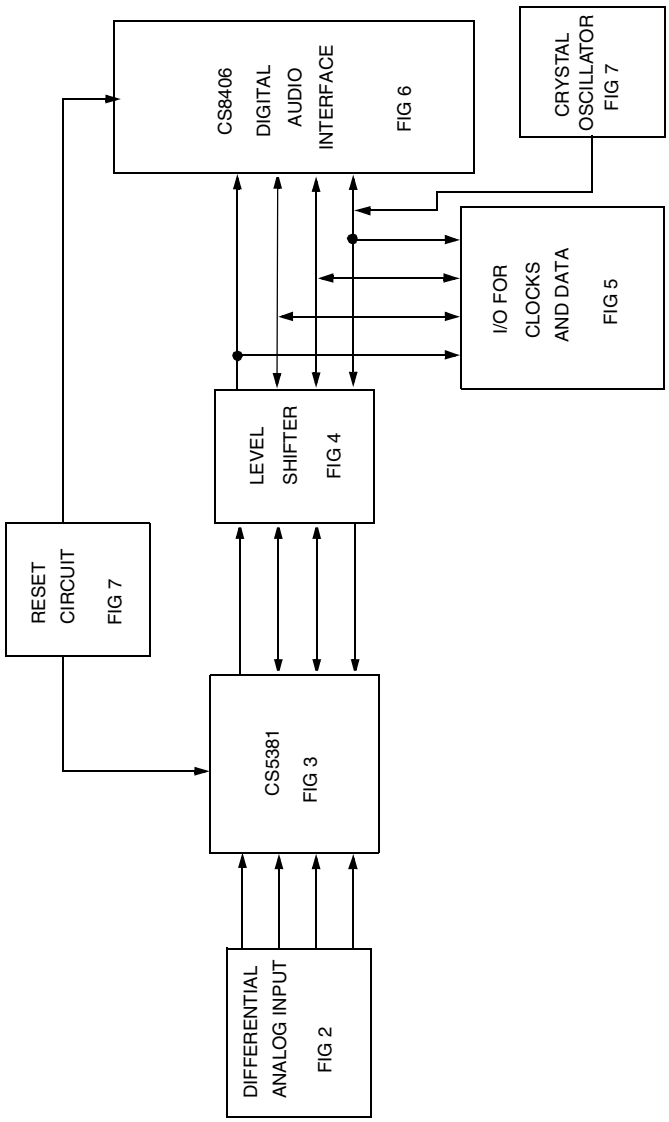

Figure 1. System Block Diagram and Signal Flow

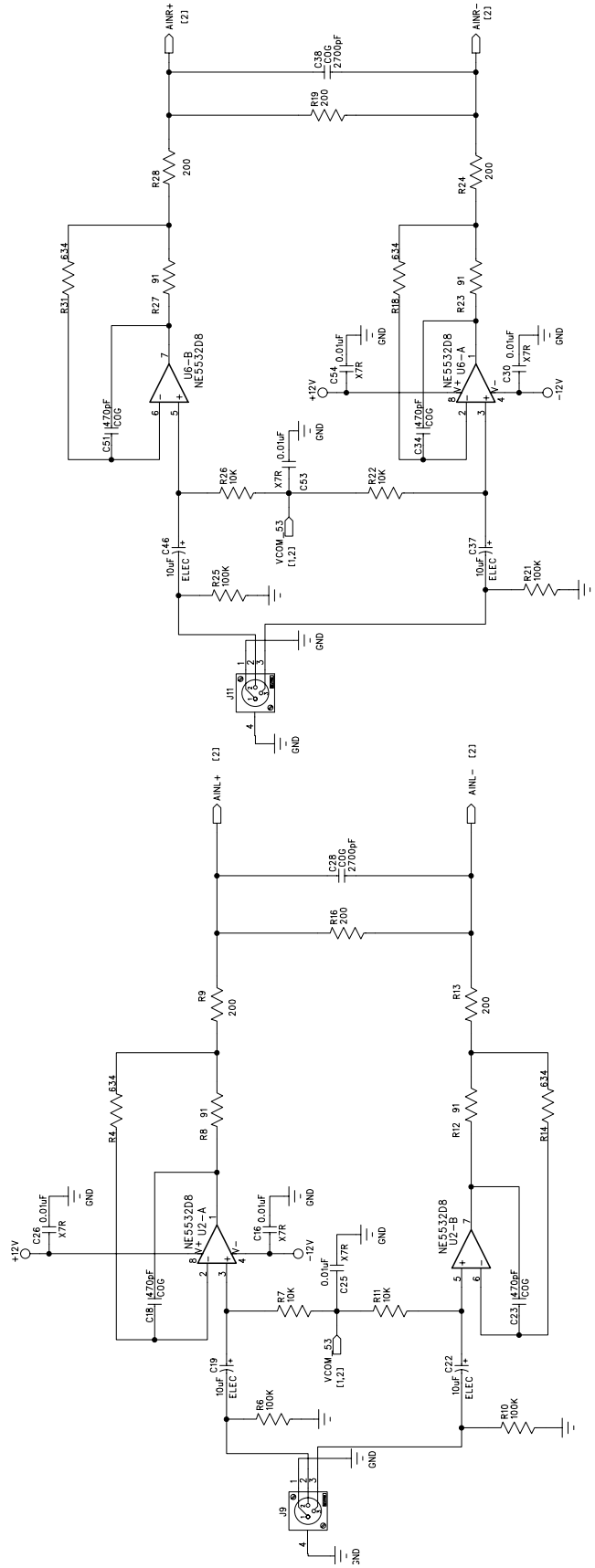

Figure 2. Differential Analog Audio Input

R9, R13, R24, R28 are 0 Ohn
R16, R19 are not installed

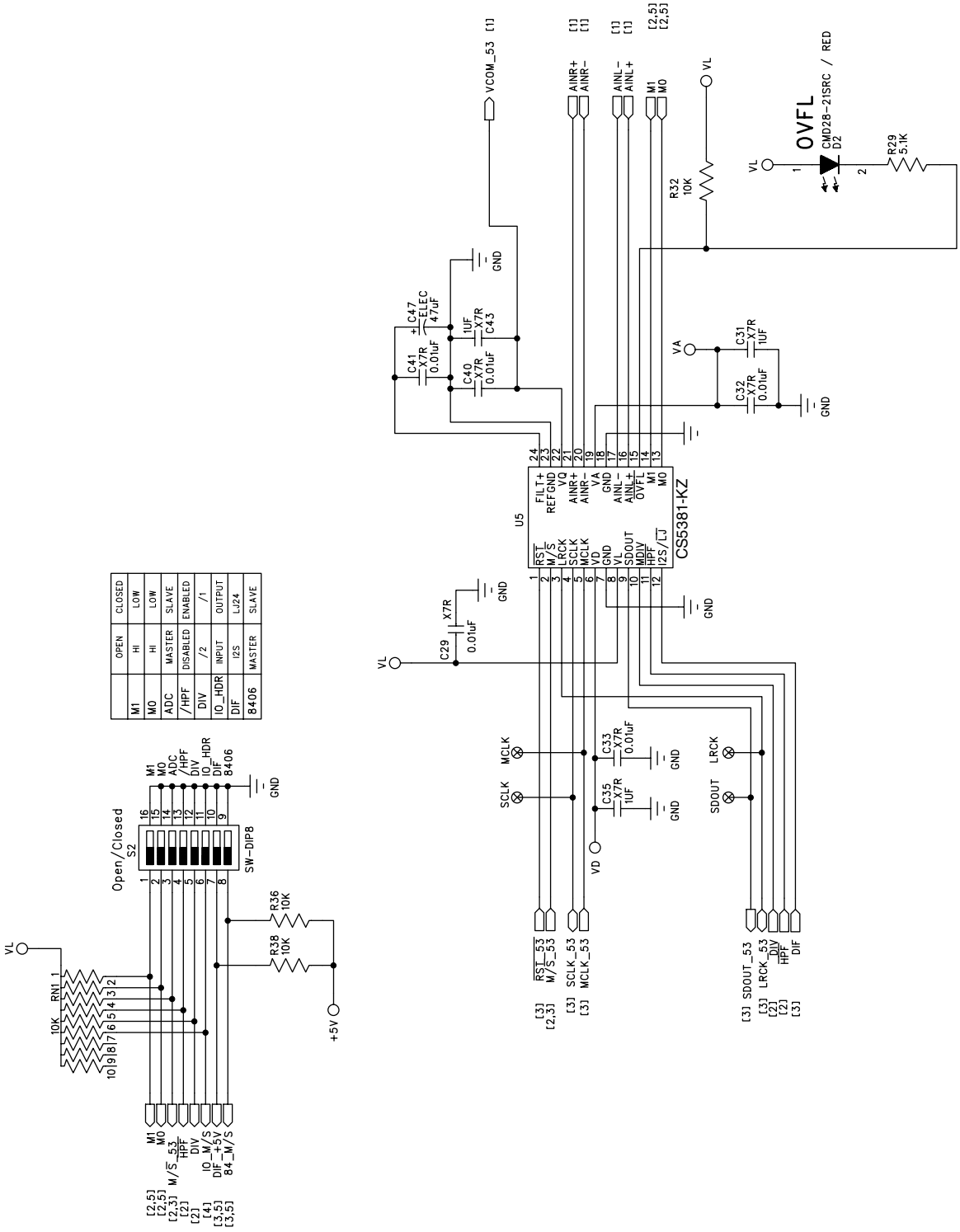

Figure 3. CS5381

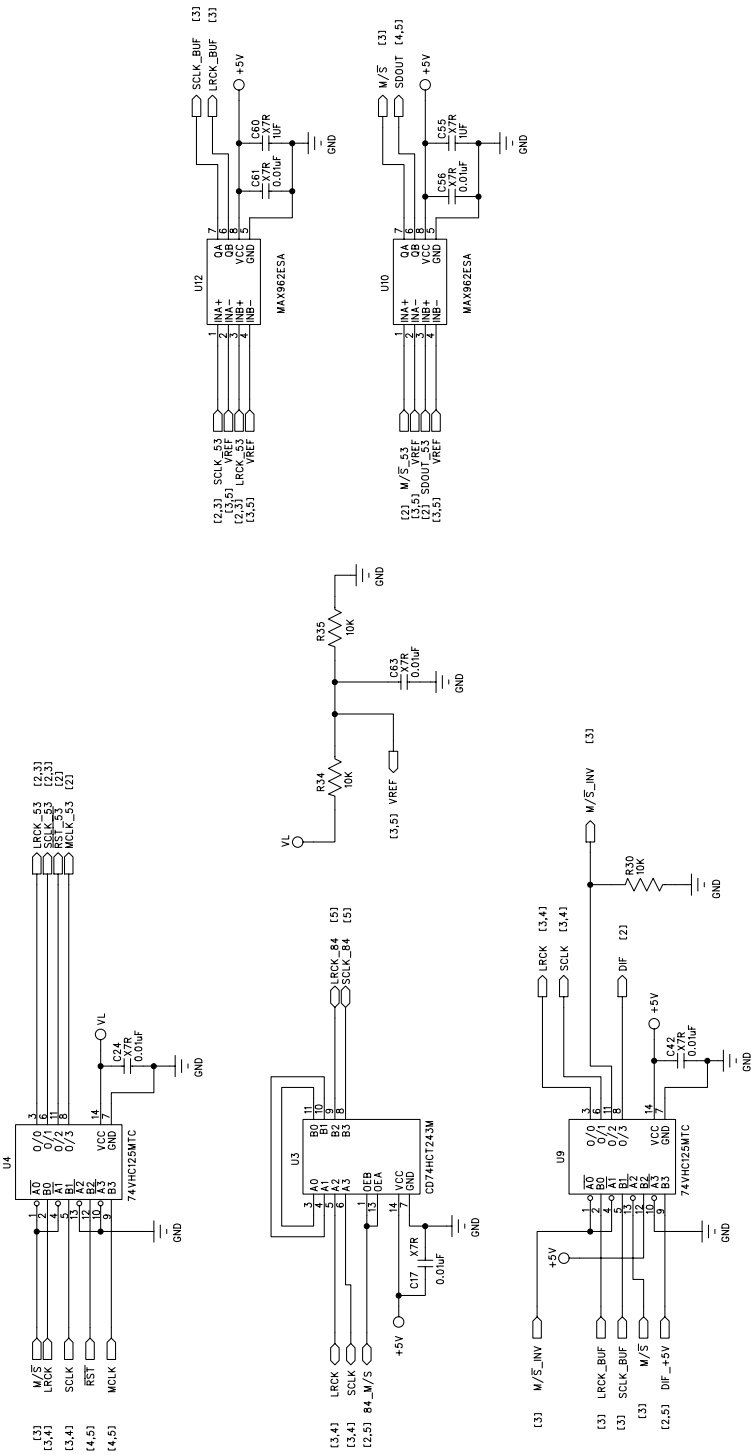

Figure 4. Level Shifters

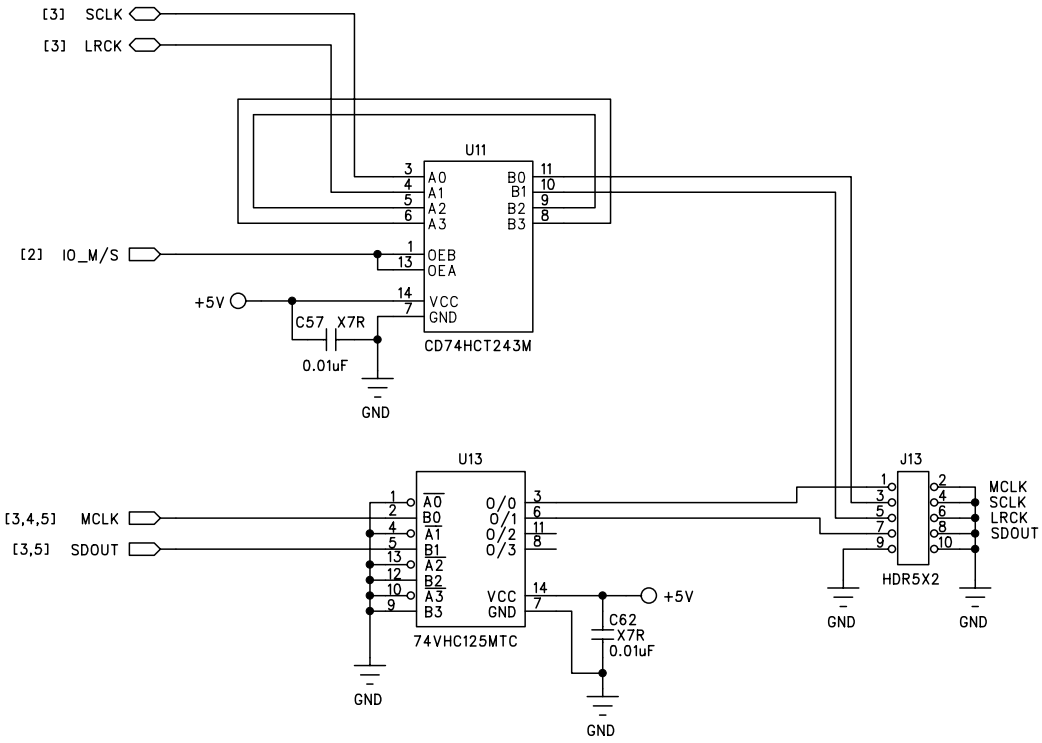

Figure 5. I/O for Clocks/Data

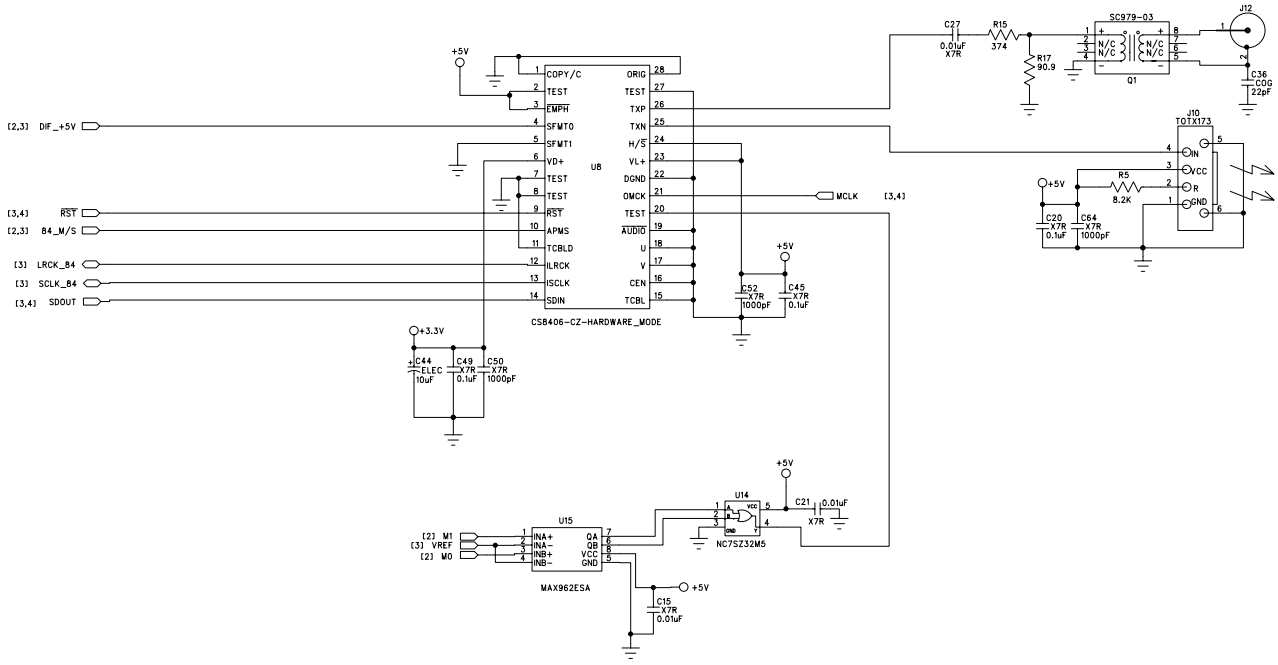

Figure 6. CS8406 Digital Audio Interface

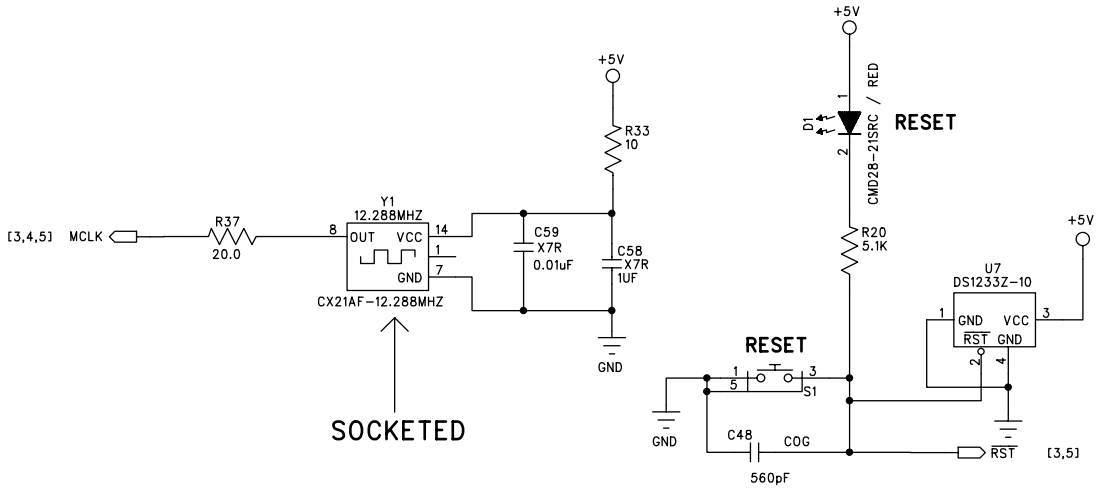

Figure 7. Reset Circuit

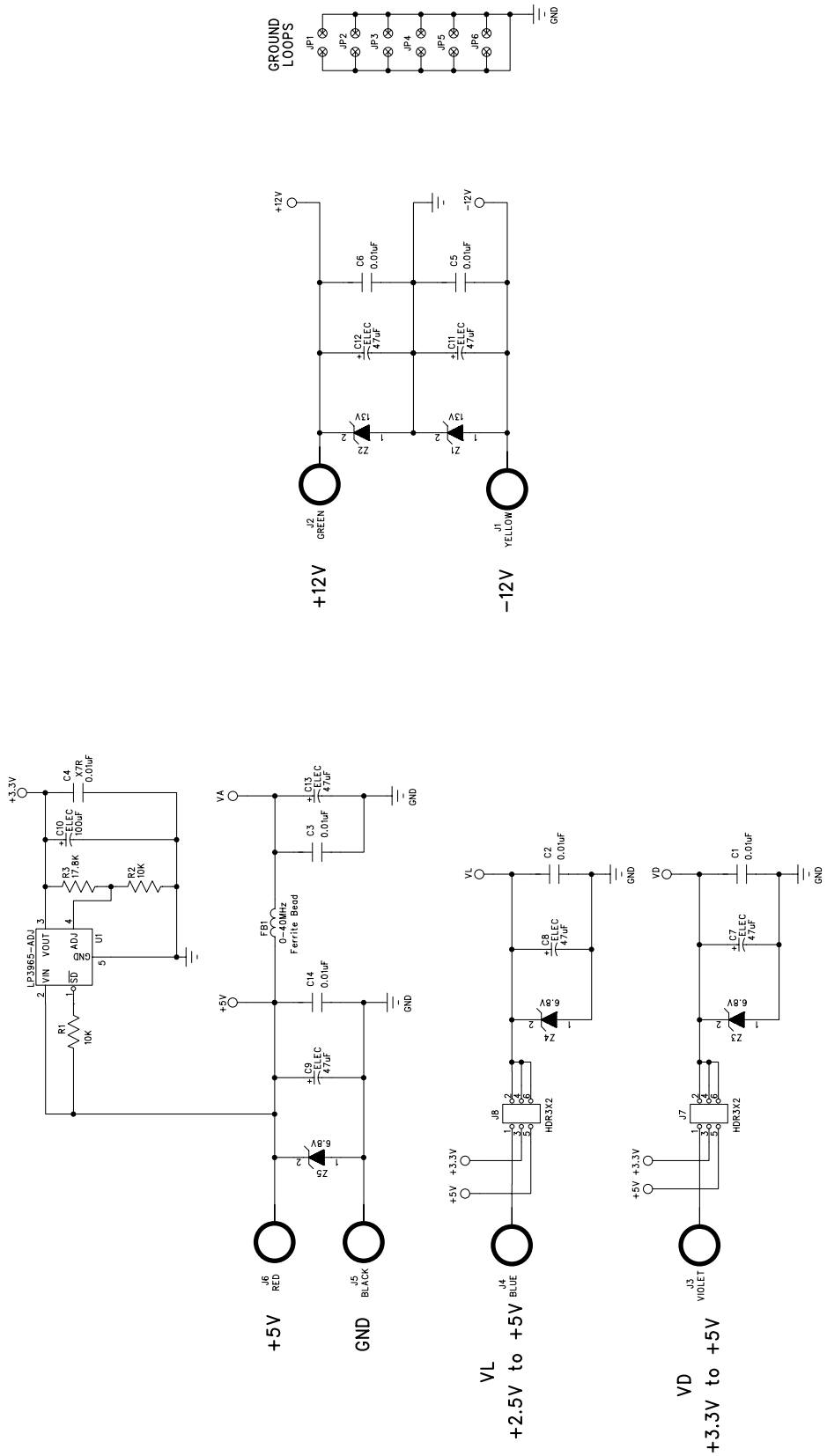

Figure 8. Power Circuit

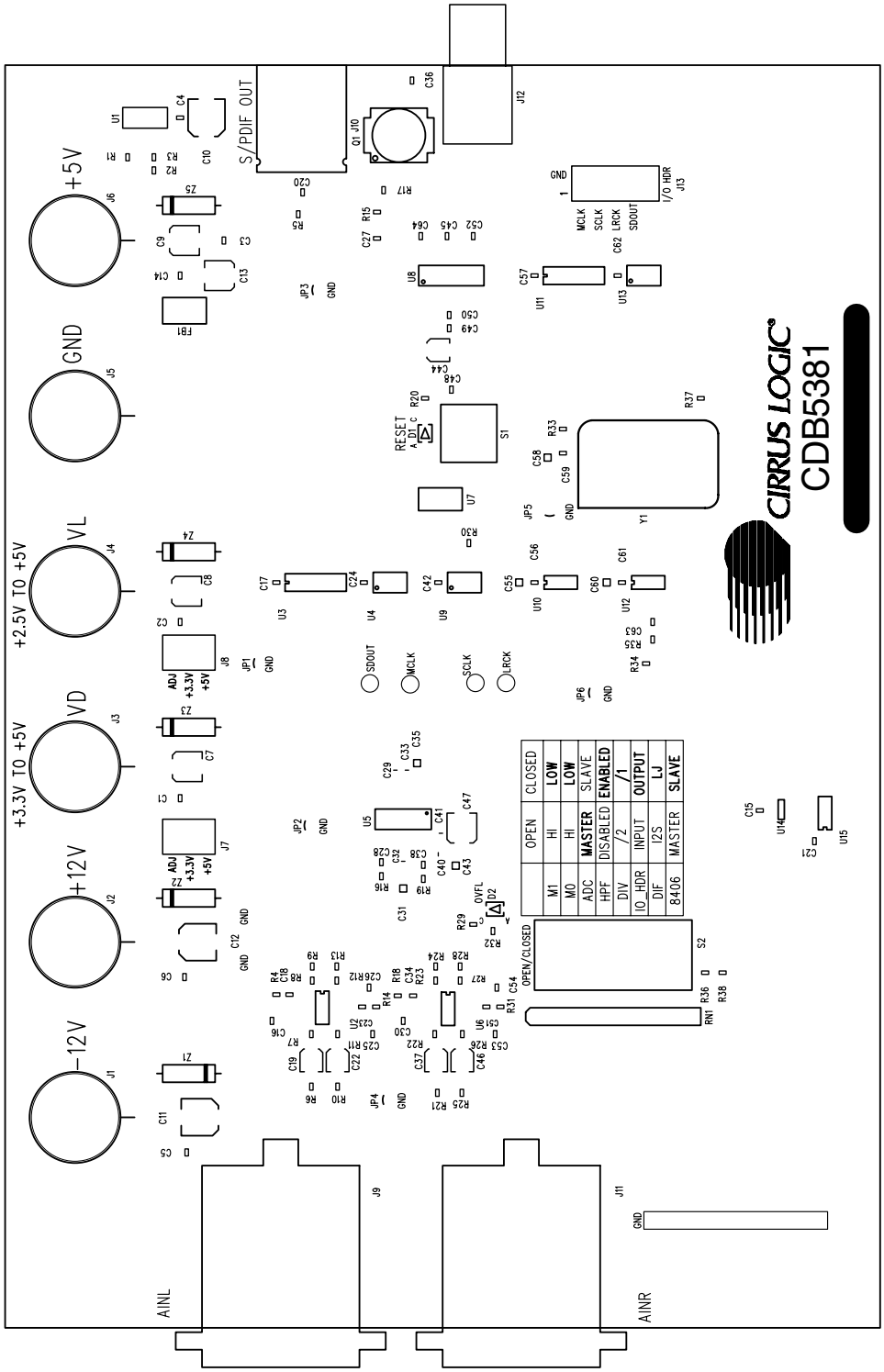

Figure 9. Top Layer Silkscreen

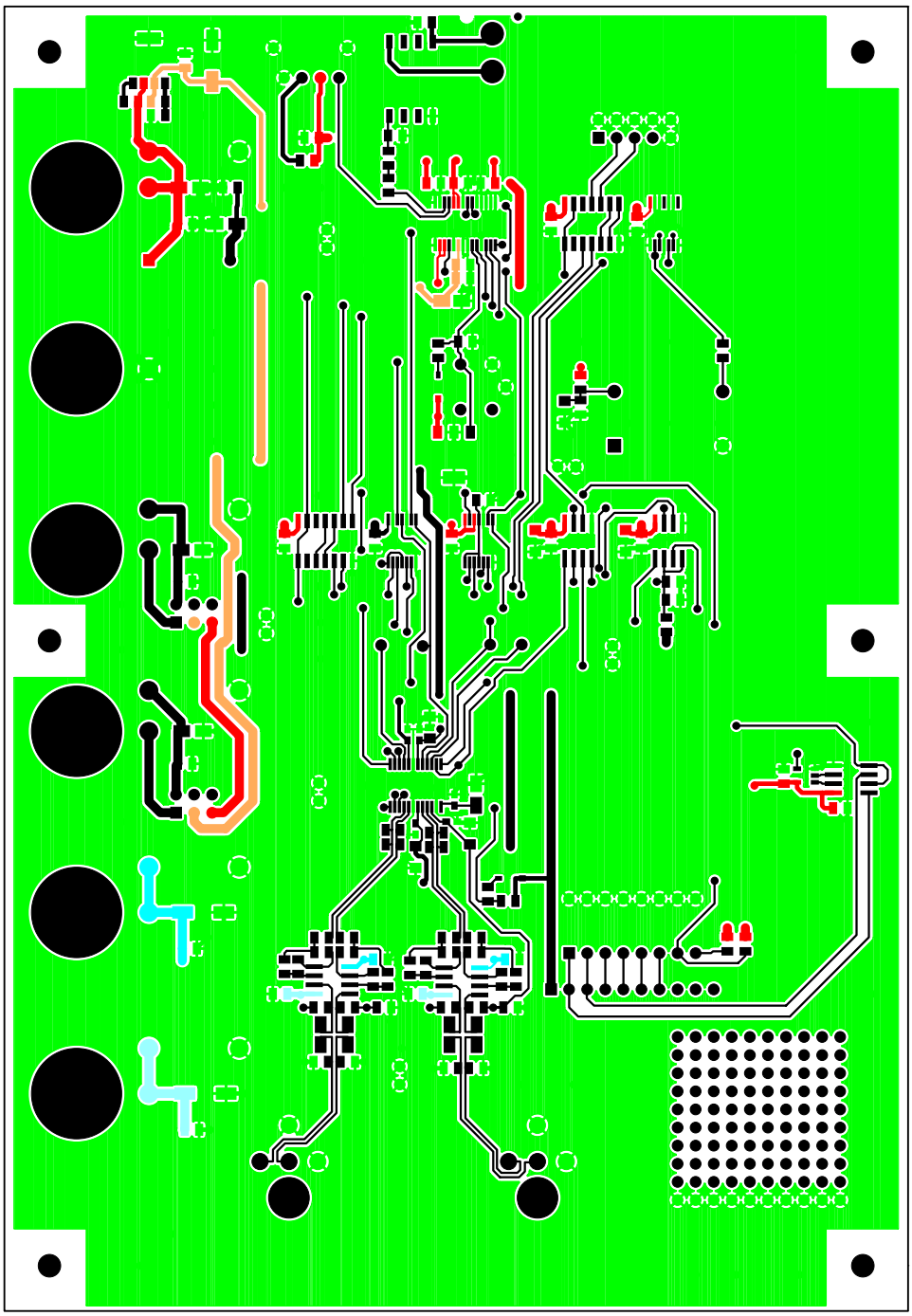

Figure 10. Top Layer

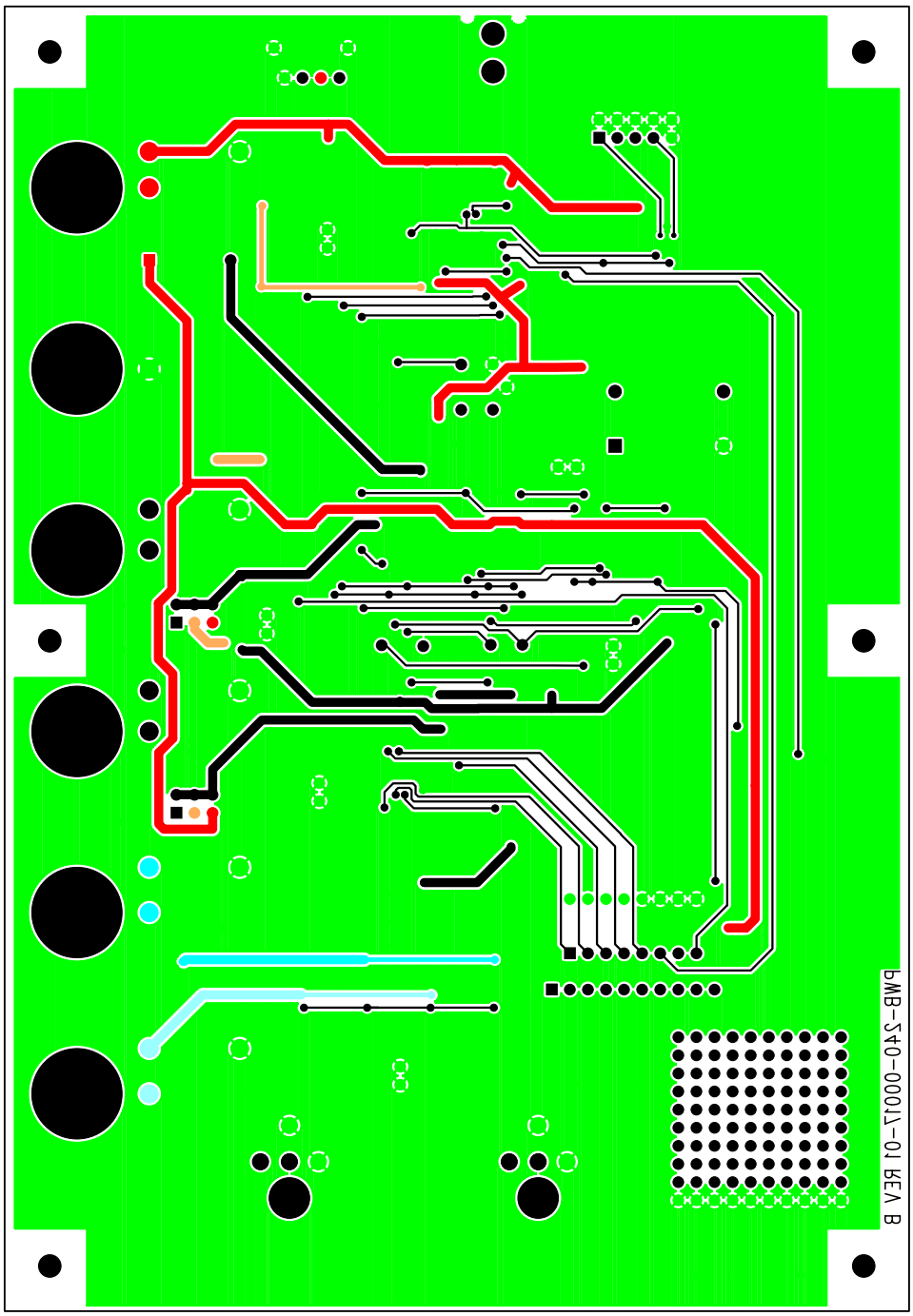

Figure 11. Bottom Layer

• Notes •


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